## REMARKS

Prior to entry of this paper, Claims 1-22 were pending. Claims 1, 16, and 20-22 were rejected. Claims 2-15 and 17-19 were identified as being allowable if re-written in independent form. In this paper, Claims 1, 2, 5, 9, 11, 14, and 22 are amended, and new Claims 23-30 are added. No new matter has been added. For at least the following reasons, Applicants respectfully submit that the presently pending claims are in condition for allowance.

### Allowable Subject Matter (Claims 2-15 and 17-19)

Claims 2-15 and 17-19 were identified as being allowable if re-written in independent form. In this paper, Claims 2, 9, 11, and 14 have been re-written in independent form. Claim 10 depends from Claim 9, Claims 12 and 13 depend on Claim 11, and Claim 15 depends on Claim 14. Accordingly, it is respectfully submitted that Claims 2 and 9-15 are in condition for allowance.

Also, it is respectfully submitted that Claim 1 is allowable at least for the reasons stated below.

For at least these reasons, it is respectfully submitted that Claim 2-15 and 17-19 are in conditions for allowance.

### Claims 20 and 21

Claims 20 and 21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hurrell (US 6,707,403) in view of Somayajula et al. (US 6,473,021) and Heim et al. (US 6,617,994). The rejection to Claims 20 and 21 is respectfully traversed.

Several different architectures for analog-to-digital conversion (ADC) are known in the art, including successive approximation ADC, sigma-delta ADC, pipeline ADC, and flash ADC.

Typically, in flash ADC, $2^k$ comparators are connected in parallel, where k represents the bits of resolution, so that parallel multi-bit conversion may be performed. In flash ADC, all of the bits are converted in parallel.

Typically, in successive approximation ADC, a single comparator is employed to weigh the applied analog input voltage against the output of a k-bit digital-to-analog converter (DAC). Using the DAC output as a reference, this process approaches the final result as a sum of k weighting steps, in which each step is a single-bit conversion. A k-bit successive approximation ADC requires

k comparison periods and will not be ready for the next bit conversion until the current one is complete.

Hurrell describes a successive approximation ADC with a calibration circuit which compensates for capacitive coupling errors. The successive approximation ADC 1 includes a capacitive DAC, which includes a most significant bit (MSB) capacitor array 4, a least significant bit (LSB) capacitive array 5, and a coupling capacitor ($C_{C1}$) coupled between the MSB array 4 and the LSB array 5. However, over-capacitance coupling and under-capacitance coupling can result in errors. Hurrell describes a successive approximation ADC 1 including a calibration circuit 49 that compensates for the over and under capacitance coupling errors. (See Col. 7, lines 2-25 of Hurrell).

Heim describes a capacitive flash ADC with a symmetric architecture. (See Col. 3, lines 46-57 of Heim).

It is respectfully submitted that Claim 20 is allowable for at least the following reasons.

First, it is respectfully submitted that Claim 20 is allowable at least because there is no motivation for the combination of Hurrell and Heim proposed in the Office Action. The Office Action states "It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate this design scheme of Heim et al. into the system of Hurrell to improve system performance and reliability because this would overcome the limitations associated with flash analog-to-digital converters." However, since Hurrell is a successive approximation ADC rather than a flash ADC, overcoming the limitations associated with flash analog-to-digital converters is irrelevant, and does not provide motivation for the combination.

Second, it is respectfully submitted that the proposed combination would change a fundamental operating principle of Hurrell. Incorporating the design scheme of Heim into Hurrell would change a fundamental operation principle of Hurrell, namely, the successive approximation ADC architecture of Hurrell, into a flash ADC architecture. Moreover, it is unclear what incorporating the design of Heim into Hurrell could possibly entail apart from discarding the circuit of Hurrell entirely and replacing it with the Heim circuit. There is no purpose in using the calibration circuit of Hurrell in Heim because the calibration circuit in Hurrell is used to compensate for capacitive coupling errors between the MSB and LSB capacitor banks of the capacitive DAC. Since the flash ADC architecture of Heim does not use a DAC, the calibration circuit of Hurrell would serve no purpose in the circuit of Heim.

Third, it is respectfully submitted that Claim 20 is allowable because neither Hurrell nor Heim, singly or in combination, teach or suggest the limitation "an interleaved conversion circuit that is interleaved", as recited in Applicants' Claim 20. Heim describes that n comparators may be used to provide n bits in parallel. However, Heim does not teach interleaving. A non-limiting example of interleaving would be using 2*n comparators to provide n bits, with the $1^{st}$ through $n^{th}$ comparators providing the n bits at time t1, using the $(n+1)^{th}$ through $(2*n)^{th}$ comparators to provide the n bits at time t2, using the $1^{st}$ through $n^{th}$ comparators to provide the n bits at time t3, and so on.

Claim 21 is respectfully submitted to be allowable at least because it depends on Claim 20, which is proposed to be allowable.

**Claims 1, 16, and 22**

Claim 1 is respectfully submitted to be allowable at least because the prior art of record, singly or in combination, does not teach, suggest, or disclose, "a conversion circuit that is included within the integrated circuit, wherein the conversion circuit includes: a comparison reference circuit that is configured to provide a plurality of references signals; and a comparison circuit that is configured to provide a plurality of comparator output signals in response to the plurality of reference signals and a comparison input signal, and wherein the comparison input signal is generated from the calibration reference signal if a calibration signal is asserted, wherein the comparison circuit includes a plurality of comparators", as recited in Applicants' Claim 1.

Claim 16 is submitted to be allowable at least because it depends on Claim 1, which is proposed to be allowable.

Claim 22 is submitted to be allowable at least for reasons similar to those stated above with regard to Claim 1.

**New Claims 23-30**

Claim 23 is respectfully submitted to be allowable at least because it depends on Claim 20, which is proposed to be allowable.

Claim 24 is respectfully submitted to be allowable at least because the prior art of record, singly or in combination, does not teach, suggest, or disclose, in combination with the other

limitations of the claim, "the calibration reference circuit includes a resistor ladder", as recited in Applicant's Claim 24.

Claim 25 is respectfully submitted to be allowable at least because the prior art of record, singly or in combination, does not teach, suggest, or disclose, in combination with the other limitations of the claim, "the comparison reference circuit includes a resistor ladder", as recited in Applicant's Claim 25.

Claim 26 is respectfully submitted to be allowable at least because the prior art of record, singly or in combination, does not teach, suggest, or disclose, "a flash or folding ADC" and "the comparison reference circuit is included in an integrated circuit", as recited in Applicant's Claim 23.

Claims 27-30 are respectfully submitted to be allowable at least because they depend on Claim 26, which is proposed to be allowable.

## Conclusion

It is respectfully submitted that each of the presently pending claims (Claims 1-30) are in condition for allowance and notification to that effect is requested. The Examiner is invited to contact Applicants' representative at the below-listed telephone number if it is believed that prosecution of this application may be assisted thereby. Although certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentably distinct. Applicants reserve the right to raise these arguments in the future.

Dated: July 19, 2005

Respectfully submitted,

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